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Multi-Level Formal Analysis

A New Direction for Fault Injection Attack?

L. Sauvage, T. Graba, T. Porteboeuf
PROOFS – September 17, 2015

Presentation Outline

Introduction, Motivation

Multi-level Formal Verification by Example

Challenge Regarding EMI Modeling

Conclusion & Perspectives

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Introduction, Motivation

Multi-level Formal Verification by Example

Challenge Regarding EMI Modeling

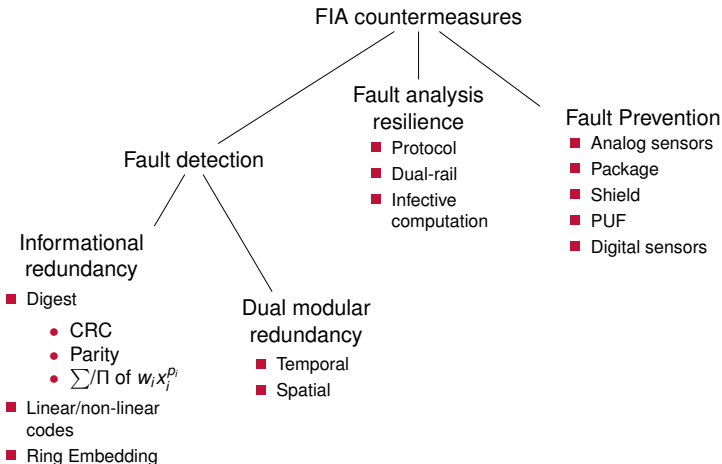Conclusion & Perspectives

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Simple & Differential Fault Analyses Are Powerful!

Number of faulted ciphertexts (C') to disclose the key

Algorithm	Key space	# C'	Fault model
RSA (CRT) [BDL97]	2^{1024}	1	Any @ S_p (or S_q)
RSA (L2R) [BDH$^+$97]		3083	Bit error @ each S&M
DES [BS97, Riv09]	2^{56}	7	Bit error @ 12th round
		9	Byte error @ 12th round
AES [PQ03]	2^{256}	4	Byte error @ 8th round
ECDSA/P-192 [BBB$^+$11]	2^{192}	36	Any in key d @ MULT

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Protections Against FIA: a Classification

FIA countermeasures

Fault analysis resilience
- Protocol
- Dual-rail
- Infective computation

Fault Prevention
- Analog sensors
- Package
- Shield
- PUF
- Digital sensors

Fault detection

Informational redundancy
- Digest
  - CRC
  - Parity
  - $\sum/\prod$ of $w_i x_i^{p_i}$
- Linear/non-linear codes
- Ring Embedding

Dual modular redundancy
- Temporal
- Spatial

Most countermeasures use fault detection with redundancy/check

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A (Short) History of Shamir's Trick

$$S = \text{CRT}(S_p, S_q) = S_q + q\Big(I_q(S_p - S_q) \bmod p\Big) \text{ with } \begin{cases} S_p = m^{d_p} \mod p, \\ S_q = m^{d_q} \mod q. \end{cases}$$

[Sha99]	Redundancy/check on S_p and S_q
[ABF$^+$02]	Redundancy/check on CRT
[YJ00]	Infective computation (no decisional test)
[YKM06]	Broken!
[KQ07]	2O-FIA attack and countermeasure
[DGRS09]	Broken! Counter-countermeasure
?	?

- Attacker underestimated: she can target operations, not only data.
- Highly time-consuming verification
  - All values (C_n^1, C_n^2, *etc.*)
  - All clock cycles
  - All order ?

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Overhead of Some Countermeasures

- Attacker overestimated: she can fault any bit (with SR $= 1$).
- Countermeasures designed to detect fault on 1+ bit
- All bits are considered, hence a high overhead

Reference	Algorithm	Countermeasure	Overhead	Non-detection
[BBK$^+$03]	AES-128	Multiple parity bits	20 %	0.12
[KKT04]	AES-128	Partially robust code	80 %	2^{-32}
[AKS12]	ECC/P-192	Nonlinear robust code	114 %	2^{-128}

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DFA   Secret extraction

Source (HDL/Soft)   ←   Countermeasure

01001101   Netlist/Inst. seq.

Platform
(FPGA/SoC)

Disturbance

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Proposal: Multi-Level Formal Analysis

DFA	Secret extraction	Faults properties
	Source (HDL/Soft) ←	Countermeasure
01001101	Netlist/Inst. seq.	Delays/placement
	Platform (FPGA/SoC)	Sensitivity
	Disturbance	Accuracy

Principle: take into account characteristics of each level

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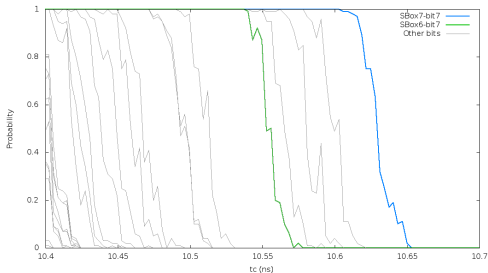
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Hardware Implementation of AES-128

Probability to be faulted of each SBox

- $Tc = 10.64$ ns: 1 bit of SBox7 is faulted
- $Tc = 10.56$ ns: SBox6&7 are faulted

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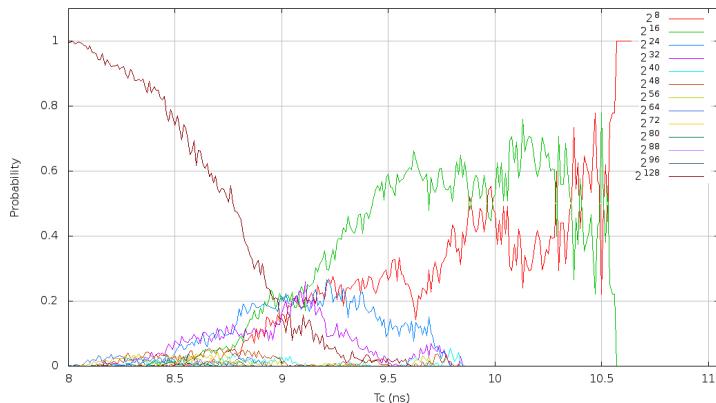TELECOM
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Hardware Implementation of AES-128
Probability to be faulted of slowest bits of SBox7 and SBox6

- Bit b faulted if it has to be updated and $t_b < Tc$
- Model complexity for verification: $16 \times 2^{2 \times 8} \times 128$ only
- Countermeasure design: SBox6-bit7 faulted highly implies SBox6-bit7 is also faulted.
- Possibility to use this information?

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Sufficient to protect only some SBoxes (instead of 16)?

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SASEBO-W/Spartan-6

16x16 array of sensors (*blue*) plus control block (*red*)

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Each sensor
is placed
into a single
configurable
logic block
(CLB).

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- $a_{12}^{(16,16)} = 1.74 \, \text{ps/dB}$
- Asymptotic standard error with linearity: 3.782 %

Impact on sensor #12 @ (x=17,y=14)

- $a_{12}^{(17,14)} = 2.11\,\text{ps/dB} > a_{12}^{(16,16)}$: greater impact
- Asymptotic standard error with linearity: 5.324 %

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Susceptibility maps: what happens outside the FPGA

- According to the EMI probe position, the delay is increased or decreased.
- The spatial distribution is not trivial (*e.g.*, Gaussian).
- Model complexity: multiplied by the number of spatial points.

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Functionnal maps: what happens inside the FPGA

- All delays are impacted

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Conclusion & Perspectives

- FIA countermeasure verification is highly time-consuming.
- FIA countermeasure overhead is high.
- Proposal take into account characteristics of each level.
- Does it help reduce verification time/overhead?

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Thanks for your attention. Any question?

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